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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,080	01/15/2004	Bruce A. Block	042390P9923D	1911

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EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,080	BLOCK ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-49* is/are pending in the application.

4a) Of the above claim(s) *25-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-24,37,38,40,41 and 44-49* is/are rejected.

7)☒ Claim(s) *39,42 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03-07-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 17 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Quek et al. (US 6,261,917).

Regarding claims 17 and 20, Quek et al. discloses a method of forming a capacitor, comprising: forming an in-laid conductor structure (20, a Cu layer. Col.2 lines 23-27) on a substrate (10); the in-laid conductor structure formed in an intra-layer dielectric (16); forming an electrode layer (a conductive layer 24 which comprises depositing TaN) (col.2 lines 28-32) directly on (it is noted that "directly on" does not mean directly contact) the conductor structure; forming a first layer (a capacitor dielectric layer 36, a deposited tantalum oxide layer. Col.3 lines 1-5) over the electrode layer; forming a second layer (a conductive layer 40) over the first layer; forming a patterned masking layer (45) over the second layer such that a potion of the second layer is exposed, and patterning the second, first and electrode layers in alignment with the masking layer, so as to form a

vertical stack superjacent the conductor; and forming a second conductor (56) over the vertical stack. Fig.4 to Fig.8.

Regarding claim 21, Quek et al. teaches that the first layer (26) is a capacitor dielectric layer which is formed of depositing tantalum oxide (col.3 lines 1-5). It is noted that tantalum oxide is known in the art as tantalum penoxide, so tantalum oxide in Quek et al.'s device is a tantalum pentoxide layer as claimed.

Regarding claims 37, 40, 41, the conductor structure (20) is considered as a first conductor structure, the electrode layer (24) is considered as a bottom electrode layer, the first layer (36) is considered as a dielectric layer, the second layer (40) is considered as a top electrode directly on the first layer, and the second conductor is considered as a second conductor structure.

Regarding claims 44, 48, the bottom electrode layer (24) comprises TaN that substantially prevents diffusion of oxygen, oxygen-containing compounds and copper.

Regarding claim 21, Quek et al. teaches that the first layer (26) is a capacitor dielectric layer which is formed of depositing tantalum oxide (col.3 lines 1-5). It is noted that tantalum oxide is known in the art as tantalum penoxide, so tantalum oxide in Quek et al.'s device is a tantalum pentoxide layer as claimed.

Claims 17, 20, 22-24, 37, 41, 44, 45, 48, and 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Adler et al. (US 6,259,128).

Regarding claims 17, 20, 22, Adler et al. discloses a method of forming a capacitor, comprising: forming an in-laid conductor structure (20, a Cu layer. Col.2 lines 45-50) on a semiconductor substrate; the in-laid conductor structure formed in an intra-layer dielectric (col.1 lines 50-61); forming an electrode layer (a conductive layer 40 , one of layers for forming capacitor plate, which comprises depositing tantalum) (col.2 lines 59-60) directly on (it is noted that "directly on" does not mean directly contact) the conductor structure; forming a first layer (a capacitor dielectric layer 70) over the first layer; forming a second layer (a conductive layer 100 is a depositing TaN) (col.2 lines 10-20) over the first layer; forming a patterned masking layer (110) over the second layer such that a potion of the second layer is exposed, and patterning the second, first and electrode layers in alignment with the masking layer, so as to form a vetical stack superjacent the conductor; and forming a second conductor (a Cu layer in a contact hole 150) (Col.4 lines 1-10) over the vertical stack including making electrical contact between the second conductor and the third layer. Fig.1 to Fig.4.

Regarding claim 23 and 24, as shown in Adler Fig.3A and Fig.4, prior the step forming the second conductor, an electrically insulating layer (120) over the second and patterning the insulating layer so as to expose portions of the second layer.

Regarding claims 37, 41, the conductor structure (20) is considered as a first conductor structure, the electrode layer (40) is considered as a bottom electrode layer, the first layer (70) is considered as a dielectric layer, the second layer (100) is considered as a top electrode directly on the first layer, and the second conductor is considered as a second conductor structure.

Regarding claims 44, 48, the bottom electrode layer (40) comprises TaN that substantially prevents diffusion of oxygen, oxygen-containing compounds and copper.

Regarding claim 45, as shown in Adler Fig.3A, the bottom electrode layer is textured (not planar).

Regarding claim 49, as shown in Adler et al.'s Fig.3A, the method further comprising: strip the patterned masking layer (photoresist layer); forming an etch stop layer (120) over exposed surfaces of ILD, bottom electrode layer, dielectric layer and top electrode layer; forming a second ILD (130) over the etch stop layer; and forming the second structure in the second ILD.

Claims 37, 40, 41, 44, and 46-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi et al. (US 6,168,991).

Regarding claims 37, 40, 41, 44, 46, 48, Ohnishi et al. discloses a method comprising: forming a first conductor structure (14) in an ILD (10); forming a bottom electrode layer (20) of TaN (col.5 lines 15-20); forming a dielectric layer (22) of Ta2O5 directly on the bottom electrode layer; forming a top electrode layer (26) of TaN (col.5 lines 20-23) directly on the dielectric layer; forming a second conductor structure (28) over the top electrode layer. See Choi et al. Fig.18.

Regarding claim 47, Choi teaches that the ILD (10) formed of silicon oxide which is known in the art as silicon dioxide. Col.3 lines 45-67).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18,19, 40, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adler et al. in view of Huang et al. (US 6,218,238).

Adler et al. Teaches all the limitations of claims 17, 20 and 22-24 as shown above and further teaches that the first layer (the capacitor dielectric layer 70) is formed of depositing silicon oxide layer (col.3 lines 1-20). Adler does not teach that the capacitor dielectric can be formed of Ta2O5.

It is conventional and also taught by Huang et al that silicon oxide and Ta2O5 are art recognized materials for forming the capacitor dielectric layer and they are interchangeable. Huang et al.'s col.3 lines 53-60.

It would have been obvious to one of ordinary skill in the art to form the capacitor dielectric layer of Ta2O5 instead of silicon oxide as taught by Huang et al. in order to have high dielectric constant capacitor dielectric layer.

Claims 37, 38, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohnishi et al. (US 6,153,460).

Ohnishi et al. discloses a method comprising: forming a first conductor structure (including layer 4 and layer 5) in an ILD (2); forming a bottom electrode layer (8) of Ru (col.4 lines 62-67 and col.5 lines 1-5) by selectively plating 9col.5 lines 1-10); forming a dielectric layer (9) directly on the bottom electrode layer; forming a top electrode layer (a Ir layer 10) directly on the dielectric layer. See Onishi et al. Fig.1(e).

Onishi et al.'s Fig.1(e) does not show a second conductor structure formed over the top electrode layer.

It is conventional as shown in Onishi et al.'s Fig.5, a second conductor structure formed over a top electrode layer (45) to connect all top electrodes together to form a common plate.

It would have been obvious to one of ordinary skill in the art to form the second conductor structure into Onishi et al.'s Fig.1(e) in order to form a common plate for memory device.

Response to Arguments

3. Applicant's arguments filed 03-07-05 have been fully considered but they are not persuasive.

Applicants argue that Quek et al. and Adler et al. do not teach the electrode layer directly on the conductior structure. In response, as clearly shown above, both

references teach the electrode layer directly on the conductor structure. It noted that "directly on" does not mean "directly contact" or "physical contact".

Allowable Subject Matter

4. Claims 39, 42, 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must

conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 872-9306. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

7. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

9. Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

5/27/05